Introduction to Boundary Scan Test and In-System Programming

Introduction

With the merger of Lattice and Vantis, the combined company has solidified its position as the top CPLD supplier with regard to in-system programmable (ISP™) devices and devices that are fully compliant to the IEEE-1149.1 testability standard. The combined Lattice and Vantis product offering includes many devices that incorporate in-system programmability through an 1149.1 compliant test access port (TAP). Devices from the ispLSI® 1000EA, 2000VE, 2000VL, 3000, 5000V, 6000, 8000/V, MACH® 4/A, MACH 5/A, ispGDXV™ and ispGDX™/A families also implement 1149.1 testability and are fully compliant with the 1149.1 standard. The devices in the ispLSI 2000E, ispLSI 2000V, ispGAL®22LV10, MACH 1SP and MACH 2SP families are offered with in-system programmability but do not include 1149.1 testability and are considered 1149.1 compatible rather than compliant.

In-system programming was developed to make it easier to use programmable logic devices packaged in fine pitch packaging, such as the PQFP or TQFP packages. A typical manufacturing flow that doesn't use ISP devices requires additional handling steps which increases the probability the delicate leads will get damaged and decreases the manufacturing yield. Over the past several years, the use of ISP devices has increased and virtually all new devices can be programmed in-system.

There are very few limitations placed on what kind of system can be used to execute an ISP device algorithm. Today, most programmable logic companies offer programming solutions which range from programming a single device through a simple cable attached to a computer, to programming several devices from different vendors as part of a board test program. Embedded programming, the ability to program devices using a microprocessor on the same board as the devices being programmed, is also readily available and gives users the ability to update the programming of a device in the field.

Benefits of ISP Through JTAG

In-system programming using a standard boundary scan test interface is necessary for compatibility with advanced board testing techniques. The IEEE 1149.1 boundary scan test interface standard, sponsored by the Joint Test Action Group (JTAG), was developed to test printed circuit board connections. The standard has been commonly referred to as JTAG. The standard also allows in-system programmable CPLDs to be programmed through the same interface used for test. The 1149.1 standard defines a simple, serial interface that allows for program and test of multiple devices using basic desktop tools. If a design incorporates 1149.1-ISP devices, then no separate programming interface is needed. All IEEE-1149.1 compatible or compliant devices (CPLDs and others) can be used in the same scan chain.

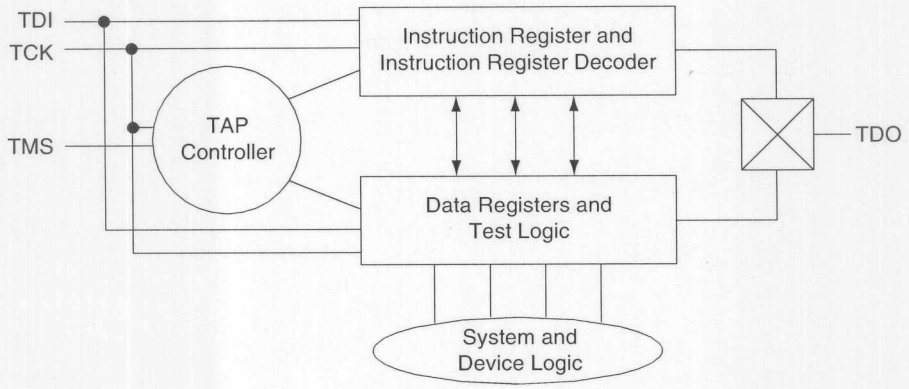
ISP devices make design jobs easier by simplifying device configuration. Designers have the option of soldering parts directly on the board and then programming them through the TAP pins. In the design phase, ISP devices let designers implement redesigns or upgrade CPLDs within a few seconds by making changes directly to devices on the board. This speeds up the design process and reduces time to market.

ISP devices also offer benefits for manufacturing. Lower inventory cost is achieved because blank devices can be used for manufacturing and then programmed at test time. This eliminates the need to maintain a separate inventory part number for each programmed part and improves the manufacturing process by facilitating board connectivity testing. Once the design is finalized and the board assembled, manufacturing engineers can use testers for both board connectivity testing and CPLD programming. As a result, 1149.1-ISP eliminates the cost of separate programming stations, unnecessary manufacturing steps and excessive handling. This shortens production time, reduces scrap cost and increases reliability.

History of the 1149.1 Standard

For years, many companies have used proprietary test methodologies implemented with boundary scan registers to reduce test complexity at the board and system level. In the late 1980's, a group of European companies formed a group with the purpose of standardizing a method for implementing and performing boundary scan testability. The composition of this group included representatives from board-test companies, system design companies and semiconductor manufacturers. A year after this group was formed, additional companies from both Asia and the United States joined this group and continued to work on a standard to be voted on by the IEEE. In 1990, this standard was passed as standard IEEE 1149.1-1990. This standard included a definition

Figure 1. IEEE 1149.1 Block Diagram



for a Test Access Port (TAP), a group of both mandatory and optional test registers, a control mechanism and timing for both the registers and TAP, and a set of both mandatory and optional test instructions. In 1993, corrections and additions were made to the standard including a language that can be used to describe its implementation in a given device. This language is called the Boundary Scan Definition Language (BSDL) and is a subset of VHDL (another IEEE standard). The 1149.1 working group continues to meet on a regular basis and constantly works to improve the standard.

What is IEEE-1149.1?

In its simplest form, the 1149.1 standard is implemented using a four pin, dedicated test access port, a 16-state, synchronous state machine, and a group of data registers. The data registers include the bypass register and a boundary scan register that is used to control the inputs and outputs of the device being tested. It also needs an instruction register and instruction register decoder that is used to control the data registers. Figure 1 shows a top-level diagram of a basic implementation of the 1149.1 standard.

There are four pins that make up the Test Access Port (TAP): TDI (Test Data Input), TMS (Test Mode Select), TCK (Test ClocK), and TDO (Test Data Output). There is an additional pin defined by the standard, $\overline{\text{TRST}}$ (Test ReSeT), which can be used to asynchronously reset both the TAP controller and the instruction register. All registers along with the TAP controller are clocked using the TCK pin.

Boundary Scan TAP Controller

The TAP Controller is a synchronous, finite state machine that controls both the TAP and the instruction and various data registers. It controls whether a device is in reset mode, where the core logic has full control of the device, if it is receiving an instruction, receiving and/or transmitting data, or is in an idle state. The state machine, as illustrated in Figure 2, is completely controlled by TMS and is clocked by TCK. The value of TMS is located next to each transition in Figure 2.

1149.1 Instructions

Where the TAP controller is the heart of any 1149.1 implementation, the instruction register and instruction register decoder can be thought of as the brains. The instruction register stores information concerning what test register or test circuitry is active. The construction of the instruction register is such that for any instruction code selected there is an associated register and/or test circuit that is also selected. This is one of the requirements stated in the 1149.1 standard. Instructions are shifted into the instruction register when the TAP controller is in the SHIFT-IR state and become active when the controller enters the UDPATE-IR state.

All Lattice/Vantis ISP devices contain three different types of instructions. The first two sets of instructions are those defined by the 1149.1 standard (required and optional). The third group of instructions is proprietary and is used to program a device. Table 1 gives a list of instructions defined in the 1149.1 standard that are implemented in the different Lattice/Vantis device families.

All of the above instructions have a unique, 5 or 6-bit code that is shifted into the instruction register. The exception to this is the BYPASS instruction that will turn on whenever its own code is selected or when an invalid code is selected.

The three required instructions each have strict requirements as to how they are expected to operate, as defined

Figure 2. TAP Controller

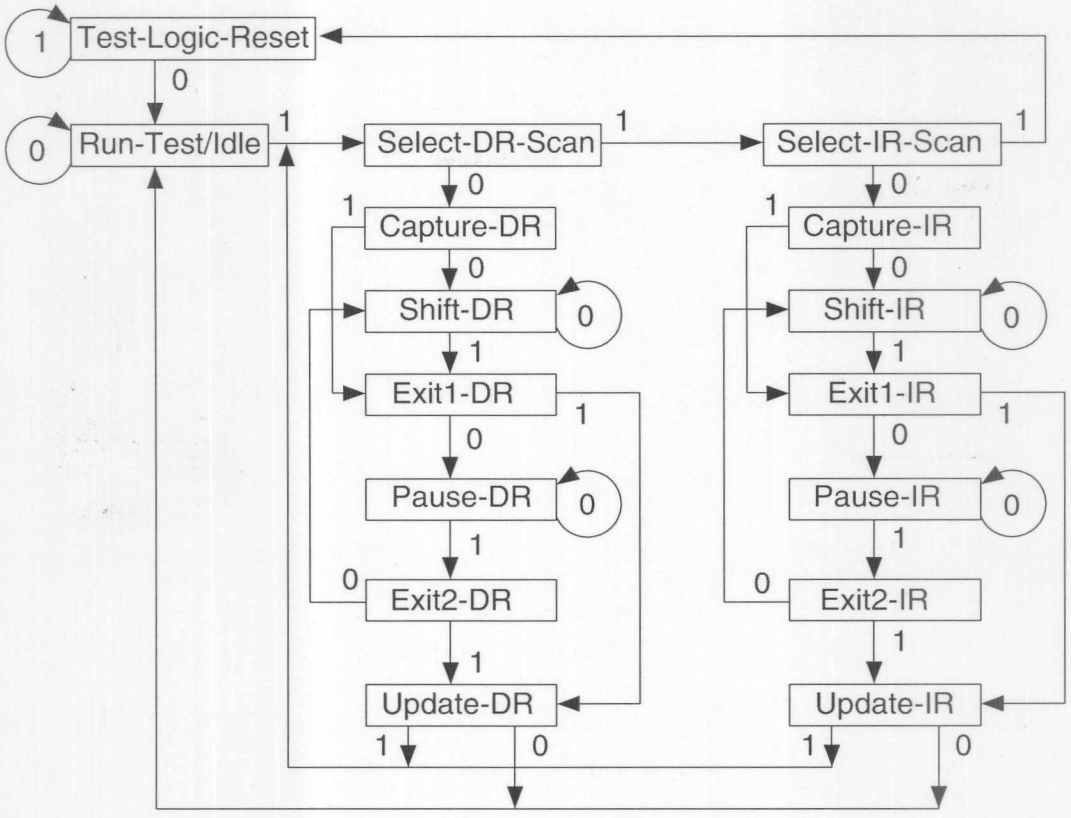


Table 1. Instructions

Boundary Scan Test Instruction	Required	Optional	ispLSI 1000EA	ispLSI 2000E	ispLSI 2000VE	ispLSI 2000V	ispLSI 2000VL	ispLSI 3000	ispLSI 5000V	ispLSI 6000	ispLSI 8000/V	MACH 1SP/2SP	MACH 4	MACH 5	ispGDXV	ispGDX/A	ispGAL22LV10
BYPASS	✓		✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓
EXTEST	✓		✓		✓		✓	✓	✓	✓	✓		✓	✓	✓	✓	
SAMPLE	✓		✓		✓		✓	✓	✓	✓	✓		✓	✓	✓	✓	
HIGHZ		✓	✓	✓	✓	✓	✓		✓		✓		✓	✓	✓		✓
IDCODE		✓	✓	✓	✓	✓	✓		✓		✓	✓	✓	✓	✓	✓	✓
USERCODE		✓	✓	✓	✓	✓	✓		✓		✓		✓		✓	✓	

in the 1149.1 standard. The BYPASS instruction enables a single-bit register, the BYPASS register, to shift data from TDI to TDO and leaves the part functioning in a normal mode. The SAMPLE instruction is used to either take a snapshot of what is happening at the I/O pins by capturing pin data into the boundary scan register or it is used to load data into the boundary scan register in preparation for an EXTEST instruction. It does this without affecting the functioning of the part. The third instruction, EXTEST, is used to perform connectivity tests by controlling the input and I/O pins of a part with the boundary scan register. EXTEST is referred to as a pin-permission instruction as it uses the boundary scan register to control the state of the I/O pins. The proprietary instructions used for programming are also pin permission instructions as the I/O pins are either tri-stated or under the control of the boundary scan registers during all programming operations.

The three optional instructions provided in Lattice/Vantis devices are also defined in the 1149.1 standard. The first of these instructions, HIGHZ, is used to tri-state all I/Os while shifting data from TDI to TDO through the BYPASS register. This instruction was included so that during programming or test operations, the I/O pins of devices not currently being accessed could be set into a "safe" state. The second instruction, IDCODE, is used to shift out a 32-bit factory signature for a device. This signature is used by both test and programming equipment to verify that the device executing instructions is the correct device type. The third optional instruction, USERCODE, is unique to devices that have some form of non-volatile memory. It is used to read out a user-programmable 32-bit device signature. The programming information for this field is included in the JEDEC file and is programmed at the same time the rest of the device is programmed.

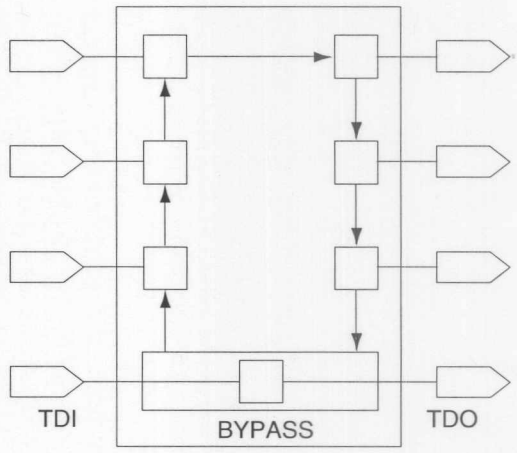
Data Registers

Two data registers have been defined by the 1149.1 standard and are considered a requirement. These are the BYPASS register and the boundary scan register (BSR). The BYPASS register is a single-bit register that is used to shift data from TDI to TDO without affecting any other circuitry. Figure 3 illustrates the BYPASS register.

The boundary scan register (BSR) is used to capture or send data from the I/O and input pins. Each boundary scan register is composed of two registers. The first register is used to either capture data from the pin or have data shifted into and out of it from the TAP. The second register is used to drive data from the first register onto an input or I/O pin. Figure 4 shows the structure of a typical BSR.

A common boundary scan register implementation uses three boundary scan control registers attached to it. The first is for the input, the second is for the output and the third is for the output enable signal. By looking at all three registers, test software can tell exactly what is happening at that I/O. If the output enable is a '1' then the I/O pin will be whatever the value of the output cell is. If the output enable is a '0,' the I/O pin is configured as an input with the value of the data in the input BSR. An input or clock pin would only have a single BSR and would not have the output tied to anything as it is used for observation only. Figure 5 shows the BSR configurations for this implementation for both the input pin and the I/O pin.

Figure 3. BYPASS Register



For a device to be considered 1149.1 compliant, it must have the TAP, TAP controller, a boundary register and the instructions BYPASS, SAMPLE, and EXTEST. A device that only has the TAP and TAP controller may be compatible with the 1149.1 standard and may work in a scan chain, but it will not be considered compliant. Any device that does not have a boundary scan register cannot be tested using the TAP because there is no means of controlling and accessing the I/O and input pins other than a direct connection. All the ispLSI 2000VE, 3000, 5000V, 6000, 8000/V, MACH 4/A, MACH 5/A, ispGDXV and ispGDX/A families are compliant with the 1149.1 standard while the ispLSI 2000E, 2000V, ispGAL22LV10, MACH 1SP and MACH 2SP families are compatible with it.

Figure 4. Boundary Scan Register

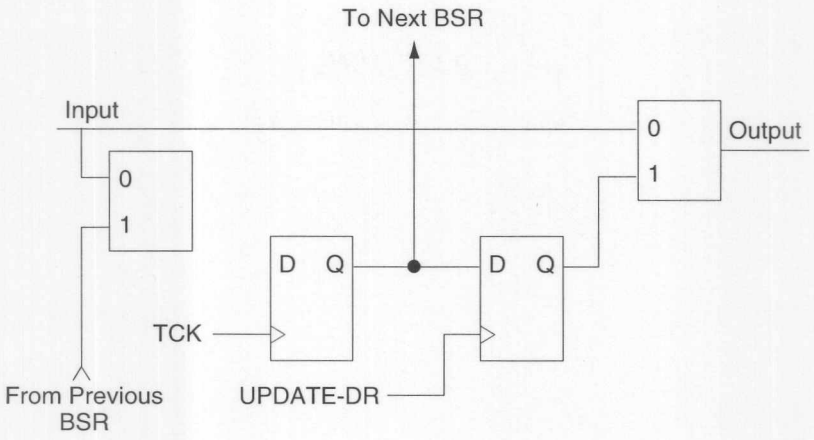


Figure 5. Common BSR Configurations